Single-Thread Processor

machine cycle	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40
PC	A	B	C	D	E	E	E	E	E	E	E	F	F	F	F	F	F	F	G	G	G	G	H	H	H	H	H	H	I	I	I	I	I	I	J	J	J	J		
FETCH		A	B	C	D	D	D	D	D	D	D	E	E	E	E	E	E	E	F	F	F	F	G	G	G	G	G	G	H	H	H	H	H	H	I	I	I	I		
DECODE			A	B	C	C	C	C	C	C	D	D	D	D	D	D	E	E	E	E	E	E	F	F	F	F	F	F	G	G	G	G	G	G	H	H	H	H	H	
OPERAND				A	B	**B**	**B**	**B**	**B**	**B**	C	**C**	**C**	**C**	**C**	**C**	D	**D**	**D**	**D**	**D**	**D**	E	**E**	**E**	**E**	**E**	**E**	F	**F**	**F**	**F**	**F**	**F**	G	**G**	**G**	**G**	**G**	**G**
EXECUTE					A						B						C						D						E						F					
ADDRESS						A						B						C						D						E						F			
MEM							A						B						C						D						E						F		
MEM								A						B						C						D						E						F	
MEM									A						B						C						D						E						F
WRITEBACK										A						B						C						D						E						**F**
memory in use							1	1	1				1	1	1				1	1	1				1	1	1				1	1	1				1	1	1	

Figure 1a

Single-Thread Processor with Data Cache

machine cycle	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40
PC	A	B	C	D	E	E	E	F	F	F	G	G	G	H	H	H	I	I	I	J	J	J	K	K	K	L	L	L	M	M	M	N	N	N	O	O	O	P	P	P
FETCH		A	B	C	D	D	D	E	E	E	F	F	F	G	G	G	H	H	H	I	I	I	J	J	J	K	K	K	L	L	L	M	M	M	N	N	N	O	O	O
DECODE			A	B	C	C	C	D	D	D	E	E	E	F	F	F	G	G	G	H	H	H	I	I	I	J	J	J	K	K	K	L	L	L	M	M	M	N	N	N
OPERAND				A	B	**B**	**B**	C	**C**	**C**	D	**D**	**D**	E	**E**	**E**	F	**F**	**F**	G	**G**	**G**	H	**H**	**H**	I	**I**	**I**	J	J	J	K	K	K	L	L	L	M	M	M
EXECUTE					A			B			C			D			E			F			G			H			I			J			K			L		
ADDRESS						A			B			C			D			E			F			G			H			I			J			K			L	
WRITEBACK							A			B			C			D			E			F			G			H			I			J			K			L

Figure 1b

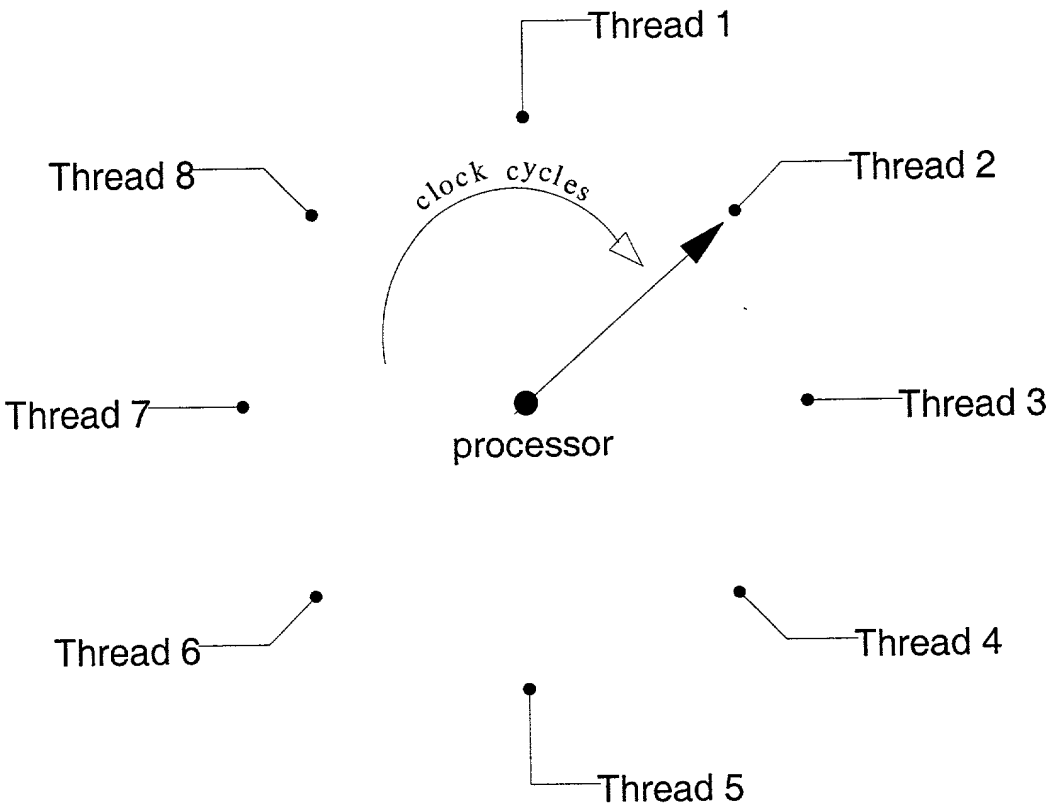

Thread 1
Thread 8
clock cycles
Thread 2
Thread 7
processor
Thread 3
Thread 6
Thread 4
Thread 5

Figure 2

Four-Thread Processor

active thread	1	2	3	4	1	2	3	4	1	2	3	4	1	2	3	4	1	2	3	4	1	2	3	4	1	2	3	4	1	2	3	4	1	2	3	4
PC	1A	2A	3A	4A	1B	2B	3B	4B	1C	2C	3B	4B	1C	2C	3C	4C	1D	2C	3C	4C	1D	2D	3D	4C	1D	2D	3D	4D	1E	2D	3D	4D	1E	2E	3E	4D	1E	2E	3E	
FETCH		1A	2A	3A	4A	1B	2B	2B	2B	2B	3B	3B	3B	4B	4B	1C	1C	1C	2C	2C	2C	2C	3C	3C	4C	4C	4C	4C	1D	1D	1D	2D	2D	3D	3D	3D	4D	4D	1E	
DECODE			1A	2A	3A	4A	1B	1B	1B	2B	2B	2B	3B	3B	3B	4B	4B	4B	1C	1C	1C	1C	2C	2C	2C	3C	3C	3C	4C	4C	4C	1D	1D	2D	2D	2D	3D	3D	4D	
OPERAND				1A	2A	3A	4A	4A	4A	1B	1B	1B	2B	2B	2B	3B	3B	3B	4B	4B	4B	1C	1C	1C	2C	2C	2C	3C	3C	3C	4C	4C	4C	1D	1D	1D	2D	2D	3D	
EXECUTE					1A	2A	3A	3A	3A	4A	4A	4A	1B	1B	1B	2B	2B	2B	3B	3B	3B	4B	4B	4B	1C	1C	1C	2C	2C	2C	3C	3C	3C	4C	4C	4C	1D	1D	2D	
ADDRESS						1A	**2A**	**2A**	2A	**3A**	**3A**	3A	**4A**	**4A**	4A	**1B**	**1B**	1B	**2B**	**2B**	2B	**3B**	**3B**	3B	**4B**	**4B**	4B	**1C**	**1C**	1C	**2C**	**2C**	2C	**3C**	**3C**	3C	**4C**	**4C**	4C	
MEM							1A			2A			3A			4A			1B			2B			3B			4B			1C			2C			3C			4C
MEM								1A			2A			3A			4A			1B			2B			3B			4B			1C			2C			3C	
MEM									1A			2A			3A			4A			1B			2B			3B			4B			1C			2C			3C
WRITEBACK										**1A**			**2A**			**3A**			**4A**			**1B**			**2B**			**3B**			**4B**			**1C**			**2C**			**3C**
memory in use							1	1	1	2	2	2	3	3	3	4	4	4	1	1	1	2	2	2	3	3	3	4	4	4	1	1	1	2	2	2	3	3	3	

Figure 3a

Four-Thread Processor with Banked Memory

active thread	1	2	3	4	1	2	3	4	1	2	3	4	1	2	3	4	1	2	3	4	1	2	3	4	1	2	3	4	1	2	3	4	1	2	3	4	1	2	3	4
PC	1A	2A	3A	4A	1B	2B	3B	4B	1C	2C	3C	4C	1D	2D	3D	4D	1D	2D	3D	4D	1E	2E	3E	4E	1F	2F	3F	4F	1F	2F	3F	4F	1G	2G	3G	4G				
FETCH		1A	2A	3A	4A	1B	2B	3B	3B	3B	4B	1C	1C	2C	3C	4C	4C	1D	2D	3D	3D	4D	4D	1E	2E	3E	3E	4E	4E	1F	2F	2F	3F	4F	4F						
DECODE			1A	2A	3A	4A	1B	2B	2B	2B	3B	4B	4B	1C	2C	3C	3C	4C	1D	2D	2D	3D	3D	4D	1E	2E	2E	3E	4E	4E	1F	1F	2F	3F	3F	4F					
OPERAND				1A	2A	3A	4A	1B	**1B**	**1B**	2B	**3B**	3B	4B	**1C**	1C	2C	**3C**	3C	4C	**1D**	1D	2D	**3D**	3D	4D	**1E**	1E	2E	**3E**	3E	4E	**1F**	1F	2F	**3F**	3F	4F			
EXECUTE					1A	2A	3A	4A	4A		1B	2B		3B	4B		1C	2C		3C	4C		1D	2D		3D	4D		1E	2E		3E	4E		1F	2F		3F	4F		
ADDRESS						1A	2A	3A	3A	4A		1B	2B		3B	4B		1C	2C		3C	4C		1D	2D		3D	4D		1E	2E		3E	4E		1F	2F		3F	4F	
MEM							1A	2A		3A	4A		1B	2B		3B	4B		1C	2C		3C	4C		1D	2D		3D	4D		1E	2E		3E	4E		1F	2F		3F
MEM								1A	2A		3A	4A		1B	2B		3B	4B		1C	2C		3C	4C		1D	2D		3D	4D		1E	2E		3E	4E		1F	2F	
MEM									1A	2A		3A	4A		1B	2B		3B	4B		1C	2C		3C	4C		1D	2D		3D	4D		1E	2E		3E	4E		1F	2F
WRITEBACK										**1A**	**2A**		**3A**	**4A**		**1B**	**2B**		**3B**	**4B**		**1C**	**2C**		**3C**	**4C**		**1D**	**2D**		**3D**	**4D**		**1E**	**2E**		**3E**	**4E**		**1F**
memory1 in use							1	1	1	3	3	3	1	1	1	3	3	3	1	1	1	3	3	3	1	1	1	3	3	3	1	1	1	3	3	3	1	1	1	3
memory2 in use								2	2	2	4	4	4	2	2	2	4	4	4	2	2	2	4	4	4	2	2	2	4	4	4	2	2	2	4	4	4	2	2	2

Figure 3b

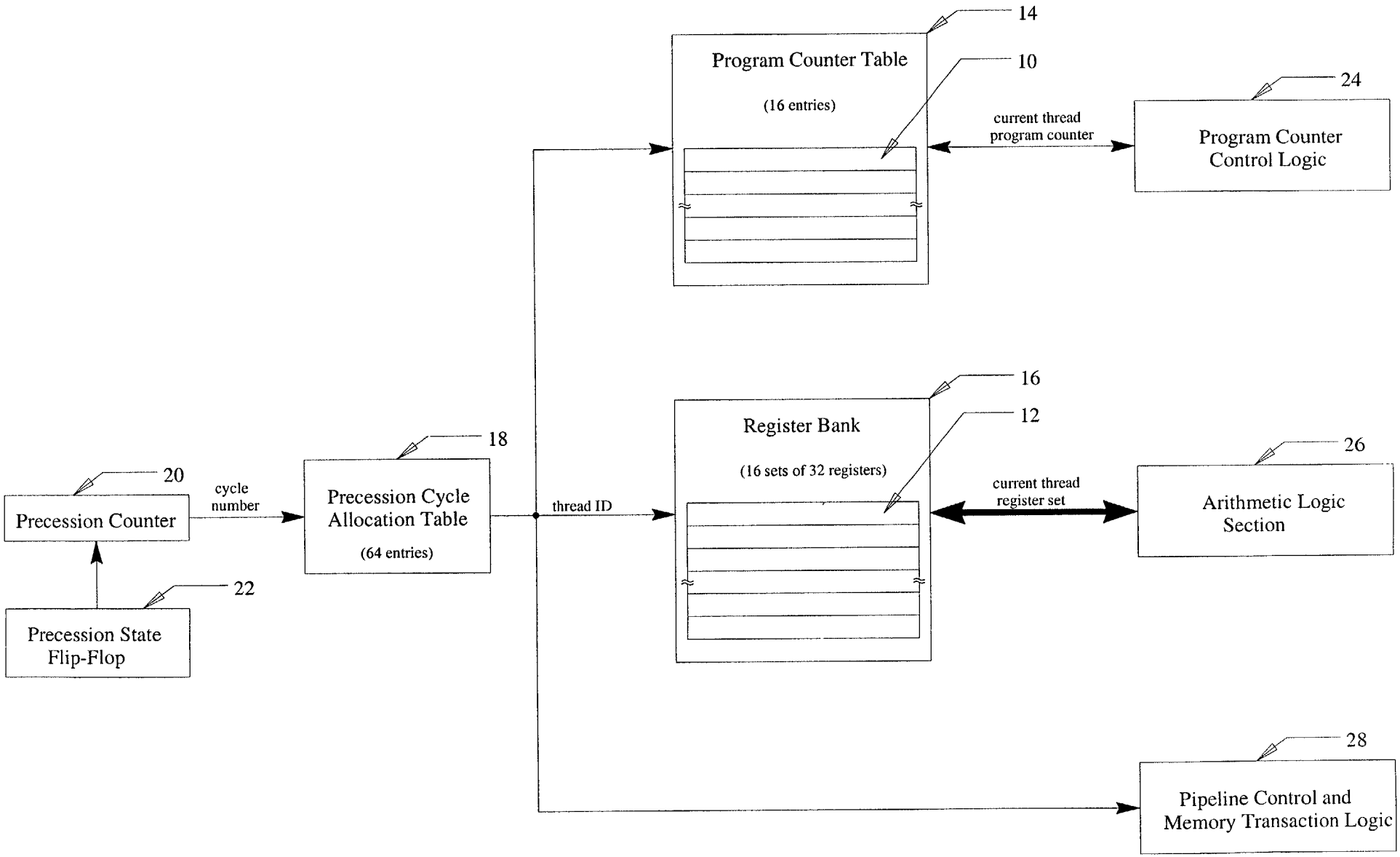
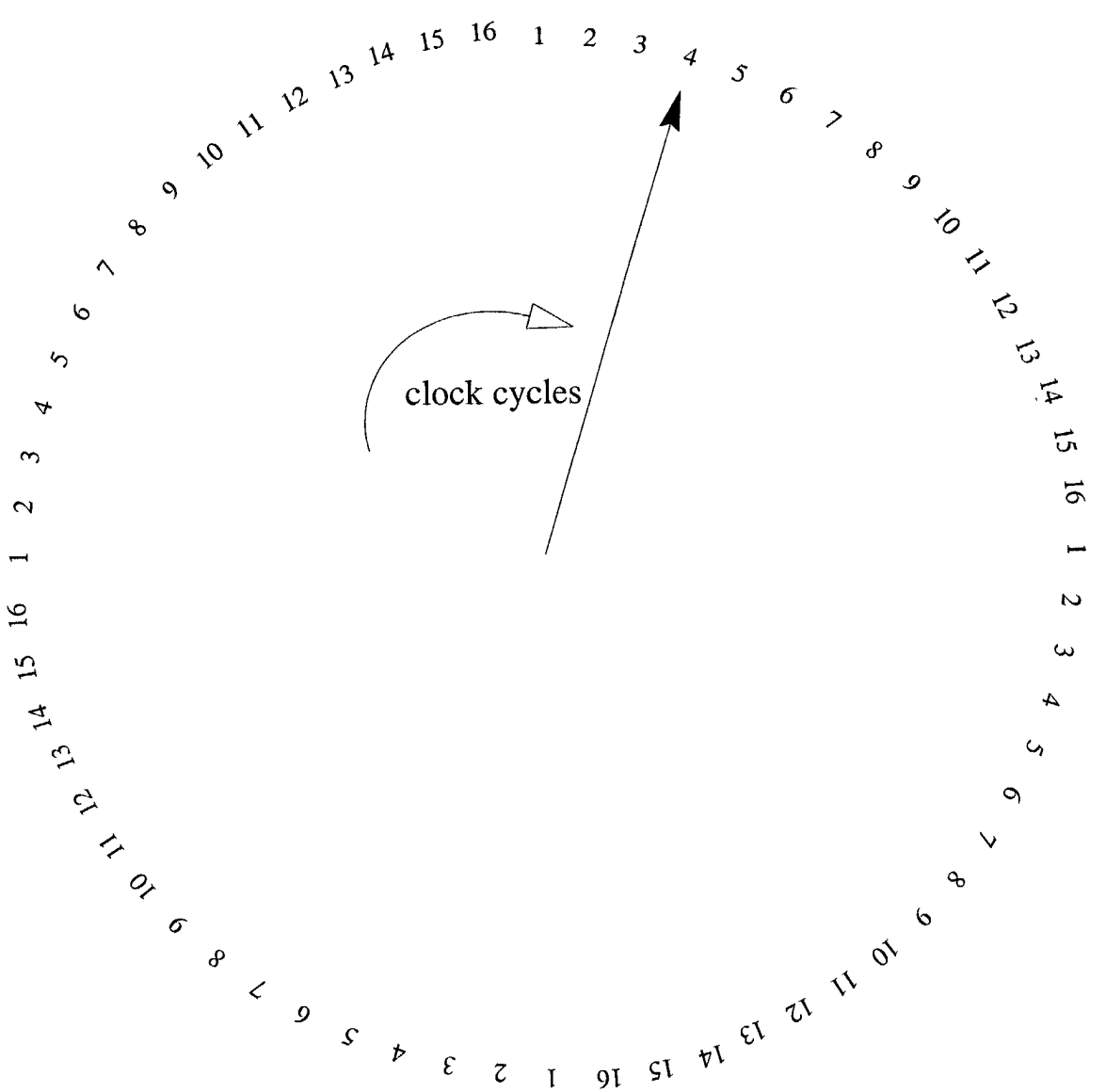

14
Program Counter Table
(16 entries)
10
24
current thread
program counter
Program Counter
Control Logic
16
Register Bank
(16 sets of 32 registers)
12
26
current thread
register set
Arithmetic Logic
Section
18
20
cycle
number
Precession Cycle
Allocation Table
(64 entries)
thread ID
Precession Counter
22
Precession State
Flip-Flop
28
Pipeline Control and
Memory Transaction Logic

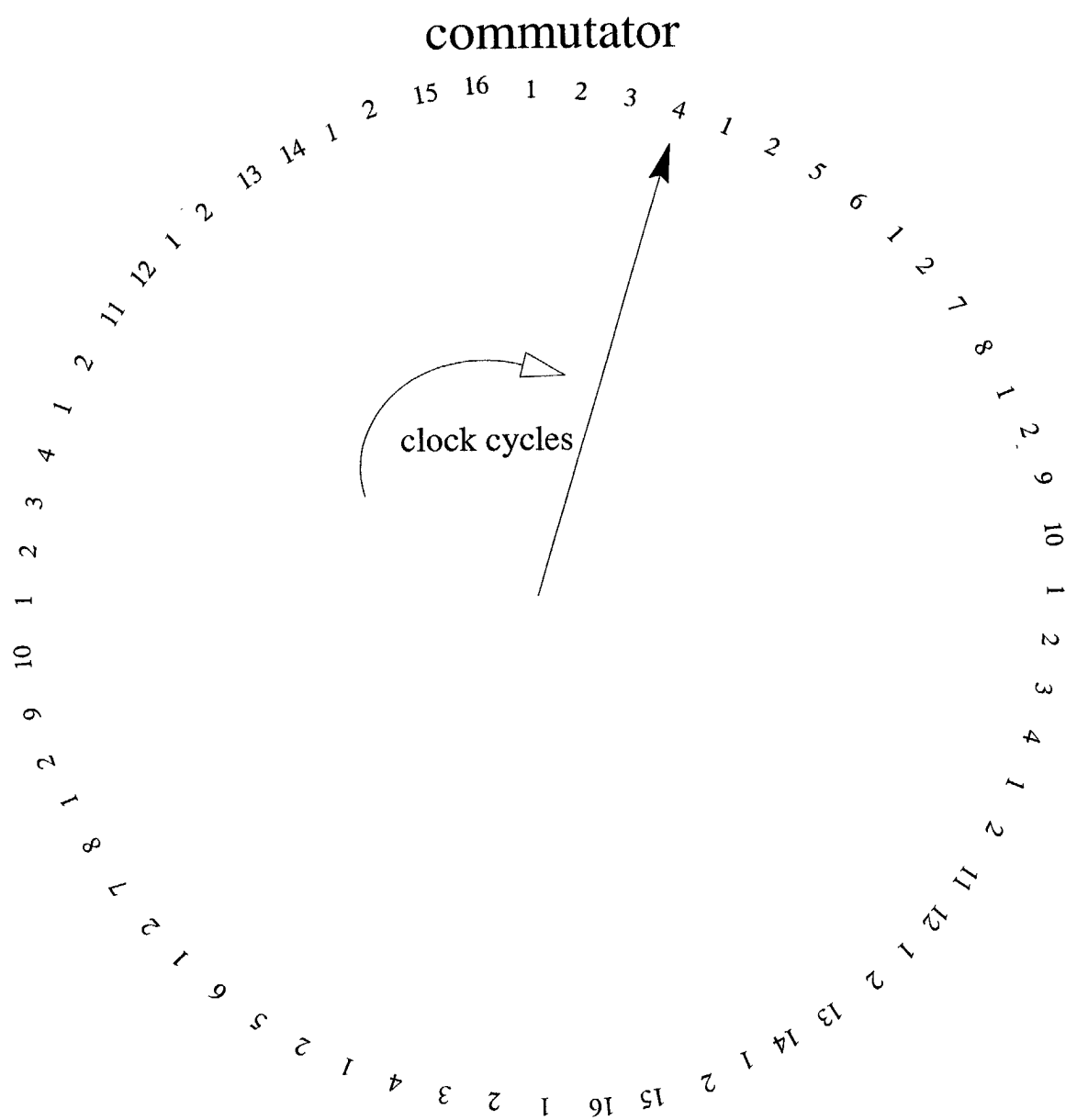
Figure 4



Cycle Allocation Table

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
⋮

Figure 5



Cycle Allocation Table

1
2
3
4
1
2
5
6
1
2
7
8
1
2
9
10
1
2
3
4
1
2
11
12
1
2
13
14
1
2
15
16
⋮

Figure 6